Name of Faculty : SATYA V.F.
Discipline : I&C
Semester : 2nd sem
Subject ADE
Lesson Plan Duration : 15 weeks(from Mar2023 to June2023)
Work Load (lecture/practical)per week (in hours) : Lectures- 03, practical- 04

Week	Theory		Practical	
	Lecture Day	Topic	Practical Day	Practical Topic
1	1	Unit:1:1.1 Concept of insulators, conductors and semiconductors, doping, minority and majority	1	To Plot V-I characteristics of a PN junction diode on bread board.
	2	charge carriers.	2	To Plot V-I characteristics of a Zener diode on bread board
	3	1.2 P and N type semiconductors , PN junction diode, mechanism of current flow in PN	3	To Plot V-I characteristics of a PN junction diode on bread board.
		junction, forward and reverse biased PN junction, potential barrier, drift and diffusion	4	To Plot V-I characteristics of a Zener diode on bread board
2	4	currents, depletion layer. V-I characteristics of diodes.	5	Observe the output of waveform using bread board: a. Half-wave rectifier circuit using one diode b. Full-wave rectifier circuit using two diodes
	5	1.3 Concept of junction capacitance in forward and reverse biased condition. Characteristics	6	Bridge-rectifier circuit using four diodes
	6	and applications of Zener diodes. Zener and avalanche breakdown.	7	Observe the output of waveform using bread board: a. Half-wave rectifier circuit using one diode b. Full-wave rectifier circuit using two diodes
		1.4 Diode as rectifier:-Diode as half-wave, full wave and bridge rectifiers. Peak Inverse	8	Bridge-rectifier circuit using four diodes

3	7	Voltage, rectification efficiencies and ripple factor calculations, Concept of filters	9	Plotting of input and output characteristics and calculation of parameters of transistors in CE configuration.
	8	Unit:2: 2.1 Concept of a bipolar transistor, its structure, PNP and NPN transistors, their symbols, Concept of leakage current.	10	Plotting of input and output characteristics and calculation of parameters of transistors in CB configuration.
	9		11	Plotting of input and output characteristics and calculation of parameters of transistors in CE configuration.
			12	Plotting of input and output characteristics and calculation of parameters of transistors in CB configuration.
4	10	Transistor as an amplifier in CE Configuration, Current amplification factors, relation b/w α, β and γ, Comparison of CB, CE and CC	13	Plotting of V-I characteristics of a FET.
	11	Unit:3: 3.1 Construction, operation and characteristics of FETs, FET as an amplifier	14	Basic logic operations AND, OR, NOT gates on bread board.
	12	3.2 Construction, operation and characteristics of a	15	Plotting of V-I characteristics of a FET.
			16	Basic logic operations AND, OR, NOT gates on bread board.
5	13	3.3 Comparison of JFET, MOSFET and BJT.	17	Verification of truth tables for NAND, NOR and Exclusive OR (EX-OR) and Exclusive NOR (EX-NOR) gates on bread board.
	14	Cl;ass test Unit :1,2,3	18	Realization of logic functions with the help of NAND or NOR gates.
	15	Unit 4: 4.1 Distinction between analogue and digital signal	19	Verification of truth tables for NAND, NOR and Exclusive OR (EX-OR) and Exclusive NOR (EX-NOR) gates on bread board.
			20	Realization of logic functions with the help of NAND or NOR gates.

6	16	4.2 Number system Decimal, Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa. Binary addition and subtraction.	21	To design a half adder using XOR and NAND gates and verification of its operations.
	17	4.3 Logic gates-Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates, NAND and NOR as universal gates.	22	Construction of a full adder circuit using XOR and NAND gates and verify its operation
	18	4.4 Gate realization with CMOS	23	To design a half adder using XOR and NAND gates and verification of its operations.
		Class test Unit:4	24	Construction of a full adder circuit using XOR and NAND gates and verify its operation
7	19	Revision	25	Verification of truth table for IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops).
	20	Revision	26	Verification of truth table for encoder and decoder ICs,
	21	Revision	27	Verification of truth table for IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops).
		Revision	28	Verification of truth table for encoder and decoder ICs,
8	22	Revision	29	Verification of truth table for Mux and De-Mux.
	23	Revision	30	Verification of truth table for Mux and De-Mux.
	24	Revision	31	viva voce
		Revision	32	viva voce
9	25	Revision	33	viva voce
		Revision	34	viva voce
	26	Unit :5: 5.1 Sequential Circuits: Half adder, Full adder,	35	viva voce
	27	Mux, De-Mux, Encoder and Decoder.	36	viva voce
	28	Combinational Circuits: Concept of latch, Flip Flops (S-R, D, J-K, T types)	37	viva voce

10	29	Basic concept of shift registers and counters.	38	viva voce
	30	A/D and D/A Converters: Basic concept of A/D and D/A converters, Applications	39	viva voce
		Revision	40	viva voce
11	31	Revision	41	viva voce
		Revision	42	viva voce
	32	Revision	43	viva voce
	33	Revision	44	viva voce
12	34	Revision	45	viva voce
	35	Revision	46	viva voce
	36	Revision	47	viva voce
		Revision	48	viva voce
13	37	Revision	49	viva voce
		Revision	50	viva voce
	38	Revision	51	viva voce
	39	Revision	52	viva voce
14	40	Revision	53	viva voce
	41	Revision	54	viva voce
	42	Revision	55	viva voce
		Revision	56	viva voce
15	43	Revision	57	viva voce
		Revision	58	viva voce
	44	Revision	59	viva voce
	45	Revision	60	viva voce