Lesson Plan

Name of Faculty : Loveleena
Discipline : I&C
Semester : 3rd sem
Subject : DE
Lesson Plan Duration : 15 weeks(from Sept 2022 to Jan 2023)
Work Load (lecture/practical)per week (in hours) : Lectures- 03, practical- 03

Week	Theory		Practical	
	Lecture Day	Topic	Practical Day	Practical Topic
1	1	Distinction between analog and digital signal.	1	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR (EXNOR) gates
	2	Applications and advantages of digital signals.	2	
	3	Binary, octal and hexadecimal number system	3	
2	4	Conversion from decimal and hexadecimal to binary and	4	Realisation of logic functions with the help of NAND or NOR gates
	5	Binary addition and subtraction including binary	5	
	6	1's and 2's complement method of	6	
3	7	Concept of code, weighted and non-weighted codes	7	To design a half adder using XOR and NAND gates and verification of its operation, Construction of a full adder circuit using XOR and NAND gates and verify its operation
	8	Examples of 8421, BCD, excess-3 and Gray code	8	
	9	Concept of parity, single and double parity and error	9	
4	10	Assignment 1	10	All files are checked
	11	Concept of negative and positive logic	11	
	12	Definition, symbols and truth tables of NOT, AND, OR,	12	
5	13	Introduction to TTL and CMOS logic families	13	Viva Voice 1
	14	Revision of sessional test 1	14	
	15	Sessional test 1	15	
6	16	Postulates of Boolean algebra, De Morgan's	16	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).
	17	Implementation of Boolean (logic) equation with gates	17	
	18	Karnaugh map (upto 4 variables)	18	
7	19	Simple application in developing combinational	19	Verification of truth table for encoder and decoder ICs, Mux and DeMux
	20	Half adder and Full adder circuit, design and	20	
	21	4 bit adder circuit	21	

8	22	Four bit decoder circuits for 7 segment display and	22	All files are checked
	23	Basic functions and block diagram of MUX and	23	
	24	Basic functions and block diagram of Encoder	24	
9	25	Concept and types of latch with their working and	25	Viva Voice 2
	26	Operation using waveforms and truth tables of RS, T, D,	26	
	27	Difference between a latch and a flip flop	27	
10	28	Assignment 2	28	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.
	29	Revision of sessional test 2		
	30	Sessional test 2	30	
11	31	Introduction to Asynchronous and Synchronous counters	31	To design a 4 bit ring counter and verify its operation
	32	Binary counters	32	
	33	Divide by N ripple counters, Decade counter, Ring counter	33	
12	34	Introduction and basic concepts including shift left	34	All files are checked
	35	Serial in parallel out, serial in serial out, parallel in serial	35	
	36	Universal shift register	36	
13	37	Working principle of A/D and D/A converters	37	Use of Asynchronous Counter ICs (7490 or 7493)
	38	Stair step Ramp A/D converter, Dual Slope,	38	
	39	Binary Weighted, R/2R ladder D/A converter	39	
14	40	Applications of A/D and D/A converter	40	All files are checked
	41	Memory organization, classification of	41	
	42	Static and dynamic RAM, Introduction to 74181 ALU	42	
15	43	Assignment 3	43	Viva Voice 3
	44	Revision of sessional test 3	44	
	45	Sessional test 3	45	